Technical Publications

Peer-Reviewed Journal Articles:

1. Mohit D. Ganeriwala, Francisco G. Ruiz, Enrique G. Marin, **Nihar R. Mohapatra**, "*A Compact model for the III-V Nanowire electrostatics including band non-parabolicty*", Journal of Computational Electronics, Accepted.

2. Apoorva Ojha and **Nihar R. Mohapatra**, "*A computationally efficient quantum-corrected Poisson solver for accurate device simulation of multi-gate FETs*", Solid State Electronics, Vol. 160, October 2019.

3. Sangya Dutta, Tanmay Chavan, **Nihar R. Mohapatra** and Udayan Ganguly, "*Electrical Tunability of Partially Depleted Silicon on Insulator (PD-SOI) Neuron*", Solid State Electronics, Vol. 160, October 2019.

4. Rohit Dawar, Samit Barai, Pardeep Kumar, Babji Srinivasan and **Nihar R. Mohapatra**, "Random forest based robust classification for lithographic hotspot detection", Journal of Micro/Nanolithography, MEMS, and MOEMS, Apr. 2019.

5. Mohit D. Ganeriwala, Francisco G. Ruiz, Enrique G. Marin, **Nihar R. Mohapatra**, A Compact Charge and Surface Potential Model for III-V Cylindrical Nanowire Transistors, IEEE Transaction on Electro Devices (IEEE TED), Vol. 66, Issue 1, pp. 73, 2019.

6. Mandar Bhoir, Yogesh Singh Chauhan and **Nihar R. Mohapatra**, Back-gate Bias and Substrate Doping influenced Substrate Effect in UTBB FD-SOI MOS Transistors: Analysis and Optimization Guidelines, IEEE Transaction on Electro Devices (IEEE TED), Vol. 66, Issue 2, pp. 861, 2019.

7. Sangya Dutta, Tinish Bhattacharya, **Nihar R Mohapatra**, Manan Suri and Udayan Ganguly, Transient Variability in SOI based LIF Neuron and Impact on Unsupervised Learning, IEEE Transaction on Electron Devices (IEEE TED), Vol 65, pp. 5137, 2018.

8. Pardeep Kumar, Babji Srinivasan and Nihar R Mohapatra, Sample Plan Selection Techniques for Lithography Process Model Building, Journal of Micro-Nanolithohraphy, MEMS and MOEMS (JM3), Vol. 17, pp. 043501, 2018.

9. Sangya Dutta, T. Chavan, S. Shukla, V. Kumar, A. Shukla, **Nihar R. Mohapatra** and Udayan Ganguly, "Dynamics, Design and Application of a Silicon-on-Insulator Technology based Neuron", MRS Advances, June 2018.

10. Pardeep Kumar, Alan E Rosenbluth, Ramana Pusuluri, Ramya Viswanathan, Babji Srinivasan and **Nihar R. Mohapatra**, "Multiple Stages of Regression to Improve Accuracy in calibrated Lithography Process", Journal of Micro Nanolithography, MEMS and MOEMS, Vol. 17, Isssue 2, pp. 023503, 2018.

11. Hari Shanker Gupta, Satyajit Mohapatra, Nisha Pandya, **Nihar R. Mohapatra**, Rohit Vasoliya and Arup Roy Chowdhury, "CFCS Calibration Circuit Design for Multi-bit Pipelined ADC Architectures", Microsystem Technologies, pp. 1, 2018.

12. Apoorva Ojha and **Nihar R. Mohapatra**, A Computationally Efficient Compact Model for Trap-Assisted Carrier Transport through Multi-stack Gate Dielectrics of HKMG nMOS transistors, Journal of Electron Devices Society (JEDS), Vol. 6, pp. 1164, 2018.

13. Mohit D. Ganeriwala, Chandan Yadav, Francisco G Ruiz, Enrique G Marin, Yogesh Singh Chauhan and **Nihar R. Mohapatra**, "Modeling of Quantum Confinement and Capacitance in III-V Gate All Around 1D Transistors", IEEE Transaction on Electron Devices, Vol. 64, Issue 12, pp. 4889, 2017.

14. Pardeep Duhan, V. Ramgopal Rao and **Nihar R. Mohapatra**, "PBTI in HKMG nMOS Transistors — Effect of Width, Layout and Other Technological Parameters", IEEE Transactions on Electron Devices, Vol. 64, Issue 10, pp. 4018-4024, October 2017.

15. Sangya Dutta, Vinay Kumar, Aditya Shukla, **Nihar R. Mohapatra** and Udayan Ganguly, "Leaky Integrate and Fire Neuron by Charge-Discharge Dynamics in Floating-Body MOSFET", Scientific Reports, Vol. 7, No. 1, Aug 2017.

16. Chandan Yadav, Mohit D. Ganeriwala, **Nihar R. Mohapatra**, Amit Agarwal and Yogesh Singh Chauhan, "Compact Modeling of Gate Capacitance in III-V Channel Quadruple-Gate FETs", IEEE Transactions on Nanotechnology, Vol. 16, Issue 4, pp. 1, July 2017.

17. Mohit D. Ganeriwala, Chandan Yadav, **Nihar R. Mohapatra**, Sourabh Khandelwal, Chenming Hu and Yogesh Singh Chauhan, "Modeling of charge and quantum capacitance in low effective mass III-V MOSFETs", Journal of Electron Devices Society, Vol. 4, No. 6, pp. 396, November 2016.

18. **Nihar R. Mohapatra**, Mohit D. Ganeriwala and Satya Siva Naresh, "Effect of pre-gate carbon implant on narrow width behavipr and performance of High-K metal gate nMOS transistors", IEEE Transaction on electron Devices, Vol. 63, July 2016.

19. Apoorva Ojha, Y. S. Chauhan and **Nihar R. Mohapatra**, "A Physics-Based Compact Model for the Threshold Voltage of Strained HKMG nMOS Transistors", Journal of Electron Devices Society, Vol. 4, Issue. 2, pp. 42, February 2016.

20. Satya Siva Naresh, Pardeep duhan and **Nihar R. Mohapatra**, "Role of Device Dimensions and Layout on the Analog Performance of Gate First HKMG NMOS Transistors", IEEE Transaction on electron Devices, Vol. 62, pp. 3792, November 2015.

21. Pardeep Duhan, Mohit Ganeriwala, V. Ramgopal Rao and **Nihar R. Mohapatra**, "Anomalous Width Dependence of Gate Current in High-K Metal Gate NMOS Transistors", IEEE Electron Device Letters, Vol. 36, Issue 8, pp.739, August 2015.

22. Pardeep Kumar, Babji Srinivasan and **Nihar R. Mohapatra**, "Fast and Accurate Lithography Simulation using Cluster Analysis in Resist Model Building", Journal of Micro/Nanolithography, MEMS, MOEMS, Vol. 14, Issue 2, pp. 023506, April-June 2015.

23. Satya Siva Naresh and **Nihar R. Mohapatra**, "Analysis and Modeling of Narrow Width Effect in Gate-First HKMG NMOS Transistors", IEEE Transaction on Electron Devices, Vol. 62, pp.1085, April 2015.

24. Amey M. Walke, **Nihar R. Mohapatra**," Effects of Small Geometries on the Performance of Gate First High-K Metal Gate NMOS Transistors", IEEE Transaction on Electron Devices, Vol. 59, Issue 10, pp.2582, October 2012.

25. V. Ramgopal Rao, **Nihar R. Mohapatra,** "Device and circuit performance issues with deeply scaled High-K MOS transistors", Journal of Semiconductor Technology and Science, Vol. 4, pp. 52-62, March 2004.

26. Deleep R. Nair, **Nihar R. Mohapatra**, S. Mahapatra, S. Shukuri and J. D. Bude, "Effect of P/E scaling on drain disturb in flash EEPROMs under CHE and CHISEL operation", IEEE Transaction on Devices and Materials Reliability, Vol. 4, Issue 1, pp. 52, March 2004.

27. **Nihar R. Mohapatra**, Deleep R. Nair, S. Mahapatra, V. Ramgopal Rao, S. Shukuri and J. D. Bude, "CHISEL Programming Operation of Scaled NOR Flash EEPROMs – Effect of Voltage Scaling, Device Scaling and Technological Parameters", IEEE Transaction on Electron Devices, Vol. 50, issue 10, pp. 2104, Oct 2003.

28. Nihar R. Mohapatra, Madhav P. Desai, Siva G. Narendra and V. Ramgopal Rao, "Modeling of Parasitic Capacitance in Deep Sub-Micrometer Conventional and High-K Gate Dielectric MOS Transistors", IEEE Transaction on Electron Devices, Vol. 50, Issue 4, pp. 959, April 2003.

29. **Nihar R. Mohapatra**, Madhav P. Desai, Siva G. Narendra and V. Ramgopal Rao, "The Impact of High-K Gate Dielectrics on Deep Sub-Micrometer CMOS Device and Circuit Performance", IEEE Transaction on Electron Devices, Vol. 49, Issue 5, pp.826, May 2002.

Peer-Reviewed Conference Proceedings:

1. Yadukrishnan M., Satyajit Mohapatra and **Nihar R. Mohapatra**, "Design and Calibration of 14-bit 10KS/s Low Power SAR ADC for Biomedical Applications", International Symposium on VLSI Design and Test, Indore, 2019 (**Best Paper Award**).

2. Satyajit Mohapatra, Hari Shanker Gupta, **Nihar R. Mohapatra**, Nisha Pandya, Sanjeev Mehta and Arup Roy Chowdhury, "A Mismatch Resilient 16-bit 20MS-s Pipelined ADC", 32nd International Conference on VLSI Design, Delhi, 2019.

3. Amratansh Gupta, Mohit D. Ganeriwala and **Nihar R. Mohapatra**, "A Unified Charge Centroid Model for Silicon and Low Effective Mass III-V Channel Double Gate MOS Transistors", 32nd International Conference on VLSI Design, Delhi, 2019.

4. Sarathchandran GM, Mohit D. Ganeriwala and **Nihar R. Mohapatra**, "Capacitance and Surface Potential Model for III-V Double-Gate MOSFETs", 2nd International Symposium on Devices, Circuits and Systems (ISDCS 2019), Hiroshima, Japan, 2019.

5. Mandar Bhoir, **Nihar R. Mohapatra**, Thomas Chiarella, Lars Ake Ragnarsson, Jerome Mitrad, Valentina Terzeiva and Naoto Horiguchi, "Effect of Sib-10nm Fin-Width on the Analog Performance of FinFETs", 3rd Electron Devices Technology and Manufacturing (EDTM) Conference 2019, Singapore, 2019.

6. Mohit D. Ganeriwala, Enrique G. Marin, Francisco G. Ruiz and **Nihar R. Mohapatra**, "A Compact Charge and Surface Potential Model for III-V Quadruple-Gate with Square Geometry", 2019 IEEE International Conference on Modeling of Systems Circuits and Devices (MOS-AK India 2019), Hyderabad, India, 2019 (**Silver Leaf Award**).

7. S. Balanethiram, S. Pande, A. K. Singh,B. Umapathi, H. S. Jatana, **Nihar R. Mohapatra** and A. Chakravorty, "Development of Low-Cost Silicon BiCMOS Technology for RF Applications", 2019 IEEE International Conference on Modeling of Systems Circuits and Devices (MOS-AK India 2019), Hyderabad, India, 2019.

8. Mohit D. Ganeriwala, Sarathchandran GM., **Nihar R. Mohapatra**, "A Simple Charge and Capacitance Compact Model for Asymmetric III-V DGFETs using CCDA", 4th IEEE International Conference on Emerging Electronics, Bangalore, 2018 (**Best Manuscript Award**).

9. Tanmay Chavan, Sangya Dutta, **Nihar R Mohapatra** and Udayan Ganguly, "An ultra-energy efficient Neuron enabled by tunnelling in sub-threshold regime on a highly manufacturable 32nm SOI CMOS technology", 76th Device Research Conference, USA, 2018.

10. Satyajit Mohapatra and Nihar R. Mohapatera, "The HotSpot Compensation in High Speed Data Converters", 61st IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Windsor, Ontario, Canada, 2018.

11. Satyajit Mohapatra, Hari Shanker Gupta and **Nihar R. Mohapatra**, "Mismatch Resilient 3.5-bit MDAC with MCS-CFCS", 2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Hong Kong SAR, China, July 2018.

12. Mohit D. Ganeriwala, Enrique G. Marin, Francisco G. Ruiz and **Nihar R. Mohapatra**, "Computationally Efficient Analytic Charge Model for III-V Cylindrical Nanowire Transistors", Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon 2018, Granada, Spain, March 2018.

13. Mandar S. Bhoir and **Nihar R. Mohapatra**, "Impact of BOX Thickness and Ground-plane on non-linearity of UTBB FDSOI MOS Transistors", Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon 2018, Granada, Spain, March 2018.

14. Subrahmanya Teja, Mandar Bhoir and **Nihar R. Mohapatra**, "Split-Gate Architecture for Higher Breakdown Voltage in STI based LDMOS Transistors", 13th IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Hsinchu, Taiwan, October 2017.

15. Neelam Surana, Joycee Mekie and **Nihar R. Mohapatra**, "Impact of High-κ Spacer on Circuit Level Performances of Junctionless FinFET", 13th IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Hsinchu, Taiwan, October 2017.

16. Jatindeep Singh, Satyajit Mohapatra and **Nihar R. Mohapatra**, "Performance Optimized 64b/66b Line Encoding Technique for High Speed SERDES Devices", 21st International Symposium on VLSI Design and Test (VDAT), Roorkee, June 2017.

17. Ashish Soni, Abhijit Umap and **Nihar R. Mohapatra**, "Low-Power Sequential Circuit Design using Work-function Engineered FinFETs", 21st International Symposium on VLSI Design and Test (VDAT), Roorkee, June 2017. **(Best Paper Award)**

18. Mandar Bhoir, Pragya Kushwaha, Yogesh S. Chauhan, and **Nihar R. Mohapatra** "Impact of substrate on the frequency behavior of trans-conductance in ultrathin body and BOX FDSOI MOS devices - a physical insight", International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), Hsinchu, Taiwan, April 2017.

19. Satyajit Mohapatra, Hari Shanker Gupta, Jatindeep Singh and **Nihar R. Mohapatra**, "A 64b/66b Line Encoding for High Speed Serializers", 30th International Conference on VLSI Design, January 2017.

20. Pragya Kushwaha, Harshit Agarwal, Yogesh Chauha, Mandar Bhoir, **Nihar R. Mohapatra,** Sourabh Khandelwal, Juan P Duarte, Yen-Kai Lin, Huan-Lin Chang, and Chenming Hu, "Predictive effective mobility model for FDSOI transistors using technology parameters", IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), University of Hong Kong, Hong Kong, HK, Aug. 2016.

21. Apoorva Ojha and **Nihar R. Mohapatra**, "An Improved model for Tunneling Probability in HKMG MOS transistors with correction in WKB Approximation", IEEE SISC, December 2016.

22. Pardeep Duhan, V. Ramgopal Rao and **Nihar R. Mohapatra**, "Width and layout dependence of HC and PBTI induced degradation in HKMG nMOS transistors", International Reliability Physics Symposium, April 2016.

23. Hari Shanker Gupta, Satyajit Mohapatra, **Nihar R. Mohapatra** and Dinesh Kumar Sharma, "Novel design of a silicon photodetector and its integration in a 4x4 CMOS pixel array", 17th International Symposium on Quality Electronics Design (ISQED), March 2016.

24. Apoorva Ojha, Narendra Parihar and **Nihar R. Mohapatra**, "Analysis and Modeling of Stress Over Layer induced Threshold Voltage shift in HKMG nMOS Transistors", 29th International Conference on VLSI Design, Kolkata, India, January 2016.

25. Pardeep Kumar, Alan E. Rosenbluth, Babji Srinivasan, Ramya Viswanathan and **Nihar R. Mohapatra**, "Lithography Process Model Building Using Locally Linear Embedding", Proceedings of International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), September 2015, Washington DC, USA.

26. Pardeep Duhan, **Nihar R. Mohapatra** and Sharad Kumar Jain, "Width Dependence of HCI and PBTI in HKMG NMOS Transistors, Proceedings of ICMAT/IUMRS, June 2015, Singapore.

27. **Nihar R. Mohapatra**, Satya Siva Naresh and Pardeep Duhan, "Analog Performance of Gate-First HKMG NMOS Transistors – Role of Device Dimensions and Layout", Proceedings of International Symposium in VLSI Technology, Systems and Applications (VLSI-TSA), April 2015, Taiwan.

28. Satyajit Mohapatra, Hari Shanker Gupta and **Nihar R. Mohapatra**, "Design of Sample and Hold for 16-bit 5MS/s Pipeline Analog to Digital Converter", Proceedings of International Conference on Emerging Technology Trends in Electronics, Communication and Networking, December 2014, NIT Surat.

29. Ashita Chandnani and **Nihar R. Mohapatra**, "Design and Analysis of Piezoresistive Polyimide Nanocantilevers for Surface Stress Sensing Applications", Proceedings of International Conference on MEMS and Sensors, Dec. 2014, IIT Madras.

30. Ritesh Jain, Holger Ruecker and **Nihar R. Mohapatra**,"Optimization of Si MOS Transistors for THz detection using TCAD simulation", Proceedings of International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), June 2014, Yokohoma.

31. Pardeep Kumar, Samit Barai, Babji Srinivasan and **Nihar R. Mohapatra**, "Process Model Accuracy Enhancement Using Cluster Based Approach", Proceedings of International Workshop on Physics of Semiconductor Devices (IWPSD), December 2013, Delhi.

32. Satya Siva Naresh, **Nihar R. Mohapatra** and Pardeep Duhan, "Effects of HfO_2 and Lanthanum capping Layer Thickness on Narrow Width Behavior of Gate First High-K Metal Gate NMOS Transistors", Proceedings of SSDM, September 2013, Fukuoka, Japan.

33. Pardeep Kumar, Babji srinivasan and **Nihar R. Mohapatra**, "Nonlinear PCA for Source Optimization in Optical Lithography", Proceedings of International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), June 2013, Glasgow, UK.

34. R. Gupta, F. Nemati, S. Robbins, K. Yang, V. Gopalakrishnan, R. Chopra, H. J. Cho, W. P. Maszara, **Nihar R. Mohapatra**, J. Wuu, D. Weiss and S. Nakib, "32nm High-Density High-Speed T-RAM Embedded Memory Technology", IEDM Technical Digest, December 2010, USA.

35. **Nihar R. Mohapatra,** R. VanBentum, E. Pruefer, W. P. Maszara, C. Calliat, Z. Chalupa, Z. Johnson and D. Fisch, "Effect of Source/Drain Asymmetry on the Performance of Z-RAM Devices", Proceedings of IEEE SOI Conference, October 2009, California, USA.

36. **Nihar R. Mohapatra**, H. Ruecker, K. E. Ehwald, R. Sorge, R. Barth, P. Schley, D. Schmidt and H. E. Wulf, "A Complimentary RF LDMOS Architecture Compatible with 0.13μm CMOS Technology", Proceedings of 18th International Symposium on Power Semiconductor Devices and ICs (ISPSD), June 2006, Naples, Italy.

37. **Nihar R. Mohapatra**, K. E. Ehwald, R. Barth, H. Ruecker, D. Bolze, P. Schley, D. Schmidt and H. E. Wulf, "The Impact of Channel Engineering on the Performance and Reliability of LDMOS transistors", Proceedings of European Solid-State Device Research Conference (ESSDERC), September 2005, Grenoble, France.

38. H. Ruecker, B. Heinemann, R. Barth, D. Bolze, J. Drews, O. Frusenko, T. Grabolla, U. Haak, W. Hoppner, D. Knoll, S. Marschmeyer, **Nihar R. Mohapatra**, H. H. Richter, P. Schley, D. Schmidt, B. Tillack, G. Weidner, D. Wolansky and H. E. Wulf, "Integration of High Performance SiGe:C HBTs with Thin-film SOI CMOS", IEDM Technical Digest, December 2004, USA.

39. Deleep R. Nair, **Nihar R. Mohapatra**, S. Mahapatra, S. Shukuri and J. D. Bude, "Effect of scaling on the reliability of flash EEPROMs under CHISEL programming", Proceedings of SISC, December 2003, Washington D.C, USA.

40. Deleep R. Nair, **Nihar R. Mohapatra**, S. Mahapatra and S. Shukuri, "The impact of technology parameters and scaling on the programming performance and drain disturb in CHISEL flash EEPROMs", Proceedings of SSDM, September 2003, Tokyo, Japan.

41. Deleep R. Nair, **Nihar R. Mohapatra**, S. Mahapatra, S. Shukuri and J. D. Bude, "The Effect of CHE and CHISEL Programming Operation on Drain Disturb in Flash EEPROMs", Proceedings of 10th International Symposium on the Physical and Failure Analysis (IPFA) of Integrated Circuits, 2003 Singapore.

42. **Nihar R. Mohapatra**, Souvik Mahapatra, V. Ramgopal Rao, S. Shukuri, "The Impact of Channel Engineering on the Performance, Reliability and Scaling of CHISEL NOR Flash EEPROMs", Proceedings of European Solid State Device Research Conference (ESSDERC), September 2003, Lisbon, Portugal.

43. D. Vinay Kumar, **Nihar R. Mohapatra**, Mahesh B. Patil and V. Ramgopal Rao, "Application of Look-up Table Approach to High-K Gate Dielectric MOS Transistor Circuits", Proceedings of 16th International Conference on VLSI Design, Jan 2003, Delhi, India.

44. **Nihar R. Mohapatra**, Souvik Mahapatra, V. Ramgopal Rao, S. Shukuri and J. D. Bude, "Effect of Programming Biases on the Reliability of CHE and CHISEL Flash EEPROMs", Proceeding of International Reliability Physics Symposium (IRPS), April 2003, Dallas, USA.

45. **Nihar R. Mohapatra**, Madhav P. Desai and V. Ramgopal Rao, "Detailed Analysis of FIBL in MOS Transistors with High-K Gate Dielectrics", Proceedings of 16th International Conference on VLSI Design, Jan 2003, Delhi, India.

46. **Nihar R. Mohapatra**, Souvik Mahapatra and V. Ramgopal Rao, "The study of Damage Generation in n-channel MOS Transistors Operated in the Substrate Enhanced Gate Current Regime", Proceedings of 9th International Symposium on the Physical and Failure Analysis (IPFA) of Integrated Circuits, 2002, Singapore.

47. **Nihar R. Mohapatra,** Madhav P. Desai, Siva G. Narendra and V. Ramgopal Rao, "Effect of technology scaling on MOS transistor performance with high-K gate dielectrics", MRS Proceedings, Vol. 716, 2002, pp. B3.3, San Fransisco, USA.

48. Krishna K. Bhuwalka, **Nihar R. Mohapatra**, Siva G. Narendra and V. Ramgopal Rao, "Effective Dielectric Thickness Scaling for high-K Gate Dielectric MOSFETs", MRS Proceedings, Vol. 716, 2002, pp. B4.19, San Fransisco, USA.

49. **Nihar R. Mohapatra**, Souvik Mahapatra and V. Ramgopal Rao, "A comparative study of scaling properties of MOS transistors in CHE and CHISEL injection", Proceedings of International Workshop on Physics of Semiconductor Devices (IWPSD), December 2001, Delhi, India.

50. **Nihar R. Mohapatra**, Souvik Mahapatra and V. Ramgopal Rao, "Study of degradation in CHISEL injection regime", Proceedings of European Solid-State Device Research Conference (ESSDERC), September 2001, Munich, Germany.

51. **Nihar R. Mohapatra**, Madhav P. Desai, Siva G. Narendra and V. Ramgopal Rao, "The impact of high-K gate dielectrics on sub 100nm CMOS circuit performance", Proceedings of European Solid-State Device Research Conference (ESSDERC), September 2001, Munich, Germany.

52. **Nihar R. Mohapatra**, Arijit Dutta, Madhav P. Desai and V. Ramgopal Rao, "Effect of Fringing Capacitance in Sub-100nm MOSFETs with high-K gate dielectrics", Proceedings of 14th International Conference on VLSI Design, Jan 2001, Bangalore, India.

List of Patents

A LATERAL DMOS TRANSISTOR AND METHOD OF FABRICATING THEREOF, Indian Patent, Application No. 201921014956, 2019.

A CURRENT SOURCE ARRAY FOR HIGH-RESOLUTION HIGH-SPEED DIGITAL TO ANALOG CONVERTERS, Indian Patent, Application No. 201821045129, 2018

METHOD OF IMPROVING MEMORY CELL DEVICE BY ION IMPLANTATION, US8431455 B2, 2013.

SOI TRANSISTOR WITH FLOATING BODY FOR INFORMATION STORAGE HAVING ASYMMETRIC DRAIN/SOURCE REGIONS, US20090242996 A1, 2009.

RAM CELL INCLUDING A TRANSISTOR WITH FLOATING BODY FOR INFORMATION STORAGE HAVING ASYMMETRIC DRAIN/SOURCE EXTENSIONS, US20090166738 A1, 2009.

RAM-Zelle mit einem Transistor mit frei einstellbarem Körperpotential zur Informationsspeicherung mit asymmetrischen Drain/Source-Erweiterungsgebieten – German Patent

SOI-Transistor mit potentialfreiem Körper für die Informationsspeicherung mit asymmetrischen Drain/Source-Gebieten – German Patent

Technical Reports Published

Feasibility of integrating Thyristor RAM (TRAM) devices into 32nm SOI CMOS Technology, GLOBALFOUNDRIES, Dresden, Germany, 2010.

Feasibility of integrating embedded DRAM (with trench capacitor) devices into 45nm SOI CMOS Technology, GLOBALFOUNDRIES, Dresden, Germany, 2010.

Feasibility of integrating Zero-capacitor RAM (ZRAM) devices into 45nm SOI CMOS Technology, GLOBALFOUNDRIES, Dresden, Germany, 2009.

Logic NVM Technology – A comparison between different IP vendors, GLOBALFOUNDRIES, Dresden, Germany, 2009.

A Complimentary RF LDMOS module for 130nm BiCMOS Technology, IHP Microelectronics, Frankfurt, Germany, 2007.

Research Grants Awarded

1. *Development of Low-Cost Bipolar Transistors for Analog and RF applications on 180nm CMOS Technology*, Science and Engineering Research Board, Department of Science and Technology, Government of India.
2. *Development of HV devices for CCD clock drivers*, Space Application Center, Indian Space Research Organization, Government of India.
3. *Cost effective integration of 20-40V n/p-LDMOS devices in SCL's 180nm CMOS process*, Department of Science and Technology, Government of India.

4. *Effects of Device Geometries and Design Rules on the Performance and Reliability of Advanced MOS Devices with High-K Gate Dielectrics and Metal Gates*, Science and Engineering Research Board, Department of Science and Technology, Government of India.

Research Guidance

- PhDs: 4 graduated, 6 ongoing
- Master students: 21 graduated, 5 ongoing

Affiliations

- Member of IEEE (Electron Devices Society, Circuits and Systems Society, Solid State Circuits Society)